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# ANALYSIS AND ESTIMATION OF AVERAGE POWER CONSUMPTION & SPEED OF A PROTOTYPE CIRCUIT BASED ON A SUM OF PRODUCT FUNCTION FOR THE DESIGN OF INTEGRATED CIRCUITS

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**ABSTRACT**

In this work the design of one combinational circuit in the form of Sum of Product (SOP) using Static & Dynamic CMOS method has been reported. The design has been carried out at 150nm channel length of MOS transistor. The functionality of the circuit has been clarified using the Tanner-SPICE software. Average power consumption, gate delay and power delay product (PDP) has been reported. The average power consumption and gate delay has been reported for the range of $V_{DD}$ from 0.5 V to 1.2 V. The comparative results of the circuit context to average power &gate delay of static CMOS and dynamic CMOS design have been presented. From the simulation results, it is found that the optimum value of PDP for the design using static and dynamic CMOS has been obtained at 0.8 V and 0.9 V respectively. The corresponding PDP values are 0.343 aJ and 0.502 aJ. Therefore, the work in this paper may be considered as prototype design for the application of high-speed & low-power VLSI circuits.

**Key Words:** Static CMOS, Dynamic CMOS, Power, Delay, PDP

## Introduction

Low power& high-speed VLSI circuit design is one of the emerging areas in the present days research [1-4]. The three major types of power dissipation in CMOS circuits are (a) switching power dissipation-$P_{SW}$ (b) short circuit power dissipation- $P_{SC}$ and (c) leakage power dissipation-$P_{LK}$[5-8]. Therefore, the total average power dissipation ($P_{AV}$) is summation of all three-power consumption. Hence, $P_{AV}= P_{SW} + P_{SC} + P_{LK}$. Among all types of power dissipation, the switching power dissipation is dominating, and it is proportional to the square of power supply voltage [1-6, 9-15]. Short circuit power dissipation is mainly dependent on rising and falling time of the input signal [1, 4-6]. On the other hand, the leakage power is due to the reverse saturation current across p-n junction [1-7] and the sub threshold current in case of a short channel device. Delay is also another metric for the design of integrated circuits [16-21].To

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enhance the portability of the circuit and to get the faster operation, reduction of power consumption and increasing of speed are the essential consideration for present days research [14-21].In this work, the average power consumption and gate delay of a combinational circuit has been measured and reported for the power supply voltage variation from 0.5 V to 1.2 V. Moreover, the CMOS static and dynamic design method has been considered to report all the results in this work.

## I. Design of Combinational Circuit based on the SOP Function

In this paper, combinational circuit has been designed using static CMOS and dynamic CMOS design style based on the function in form (SOP).The function is$Y = \overline{ABC + D}$.

The characteristics table of the function is as follows.

**Table 1. Characteristics Table of the Function $= \overline{ABC + D}$**

| **Input** | | | | **Output $Y = \overline{ABC + D}$** |
|---|---|---|---|---|
| **A** | **B** | **C** | **D** | |
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 |

### IIA. Designing of the Circuit using Static CMOS Method

Schematic diagram of the circuit using Static CMOS design based on the function (Y) $= \overline{ABC + D}$has been presented in Fig.1. As shown in Fig.1, three NMOS transistor with input terminal A, B, C respectively are connected in series in the Pull-down Network (PDN), In the PDN, the NMOS transistor, having input D, is connected in parallel with series connected transistor (A, B, C). As per CMOS design rules ,three PMOS

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transistors with input A, B, C respectively are connected in parallel at Pull-up Network (PUN) and PMOS with input D is connected is series with parallel combination of three PMOS (A, B, C) transistor at PUN. Terminal, Y is used for the output terminal. Four number of Bit sources are used to generate bit stream for the corresponding input terminal of transistors.

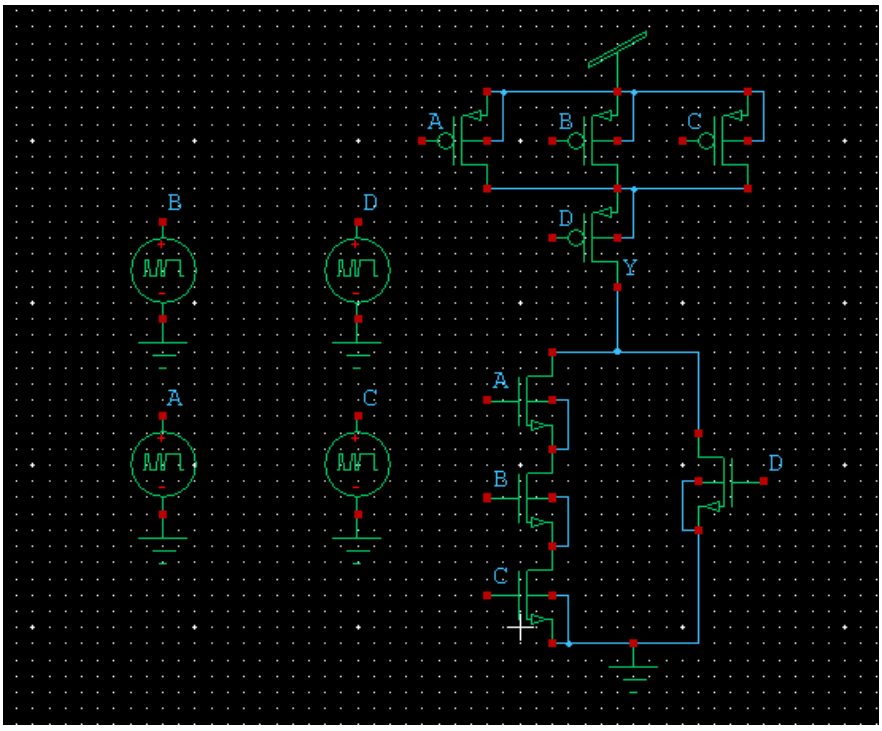


**Fig.1: Schematic diagram of the circuit using Static CMOS design based on the function (Y) $= \overline{ABC + D}$**

The circuit of Fig.1 has been simulated for the clarification of functionality with the help of T-SPICE software. The simulated input and output waveforms are shown in Fig. 2. The waveforms are validated context to the characteristics table (Table-1). This indicates the correctness of the design. The waveform related to instantaneous power dissipation is shown in Fig.3.

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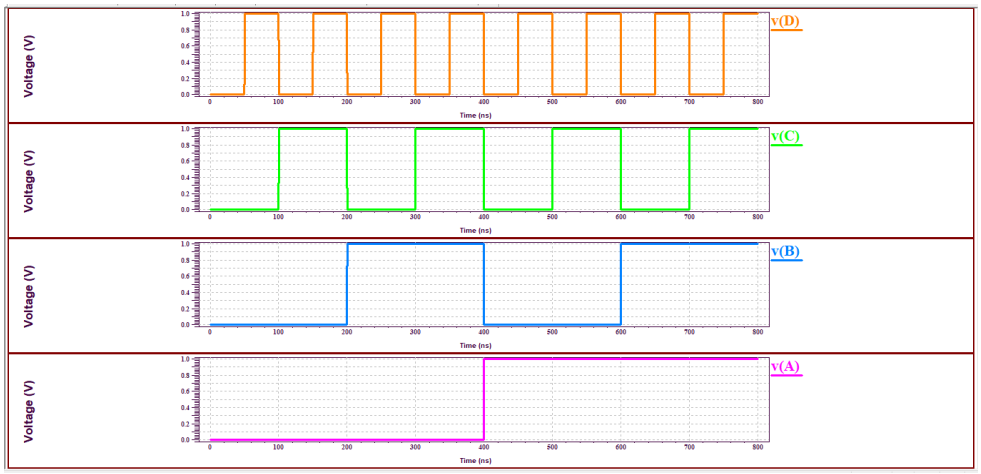


**Fig.2a: Waveforms corresponds to theinput A. B, C, D**

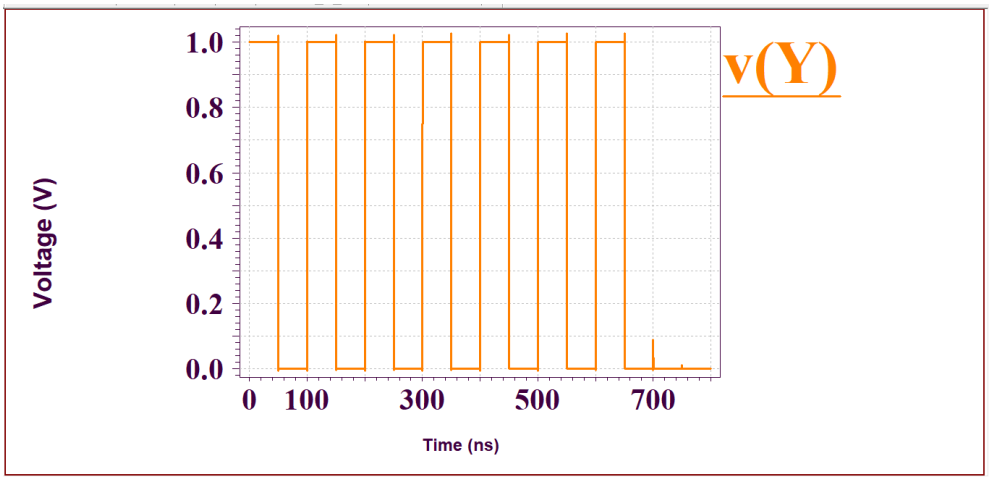


**Fig.2b: Output waveform at node Y for static CMOS design**

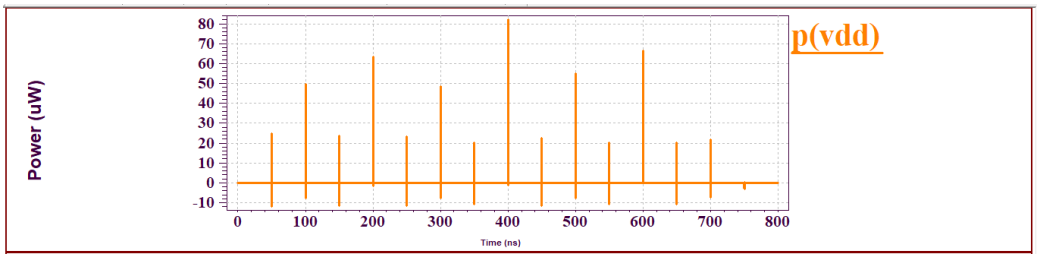


**Fig.3: Instantaneous power dissipation of the static CMOS circuit for the function Y = $\overline{ABC + D}$**

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### IIB. Designing of the Circuit using Dynamic CMOS Method

The circuit diagram of the function Y= $\overline{ABC+D}$ has been shown in Fig.4. The circuit has been design considering dynamic CMOS design style. In this design the number transistors have been reduced to 6 from 8(required in static CMOS design). The clock signal is connected to pre-charge transistor (PMOS) and evaluation transistor (NMOS). Whenever, clock signal is at low (logic zero) value, pre-charge operation takes place and output node Y is pre-charged to logic high. On the other hand, during high value of clock period, evaluation phase takes place. During evaluation phase, input signal is applied, and desired output is obtained.

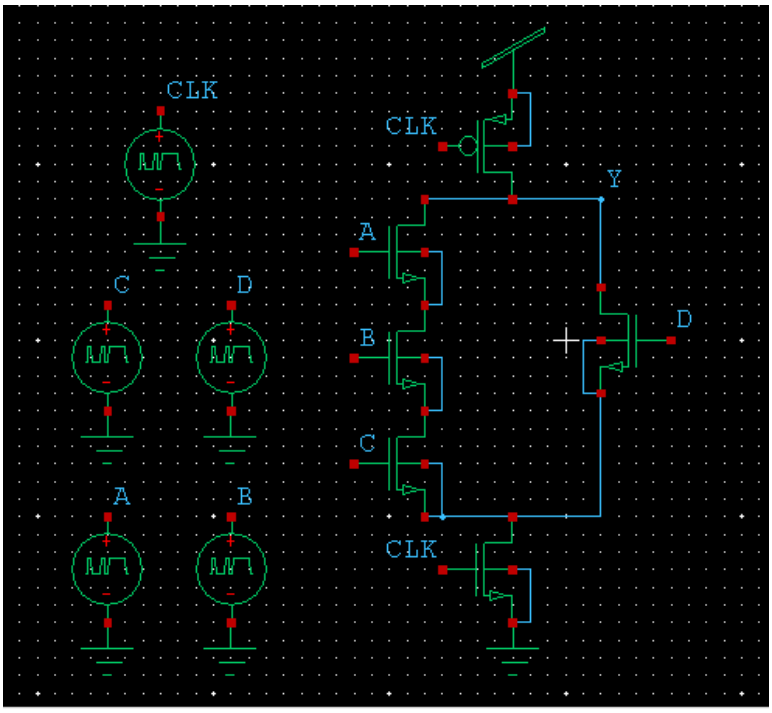


**Fig.4: Circuit diagram using dynamic CMOS method forthe function (Y) = $\overline{ABC+D}$**

The circuit of Fig.4 has been simulated with the help of T-SPICE software. The input and output waveforms are shown in Fig.5. The functionality of the design has been clarified from the output waveform reference to the characteristics table (Table-1).The nature of instantaneous power dissipation of the circuit is shown in Fig.6.

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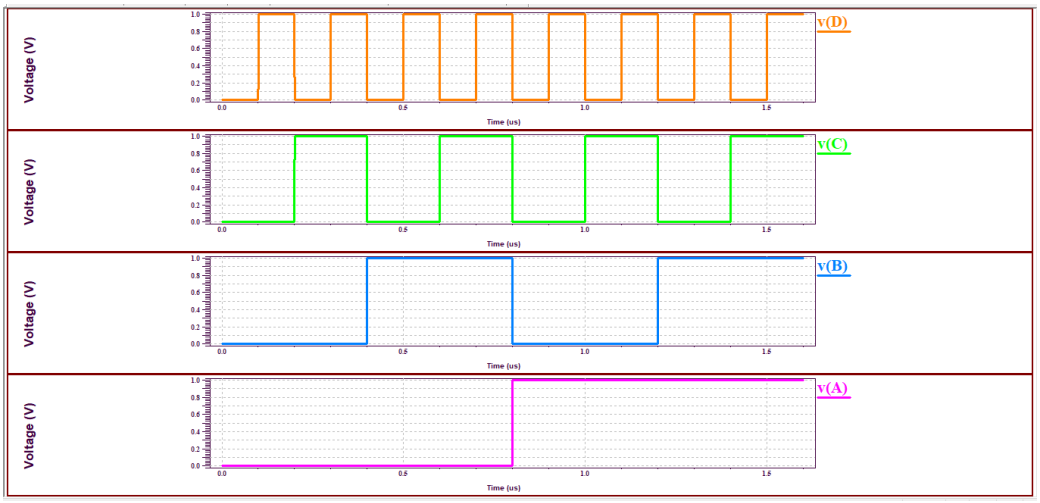


**Fig.5a: Waveforms corresponds to the input A. B, C, D**

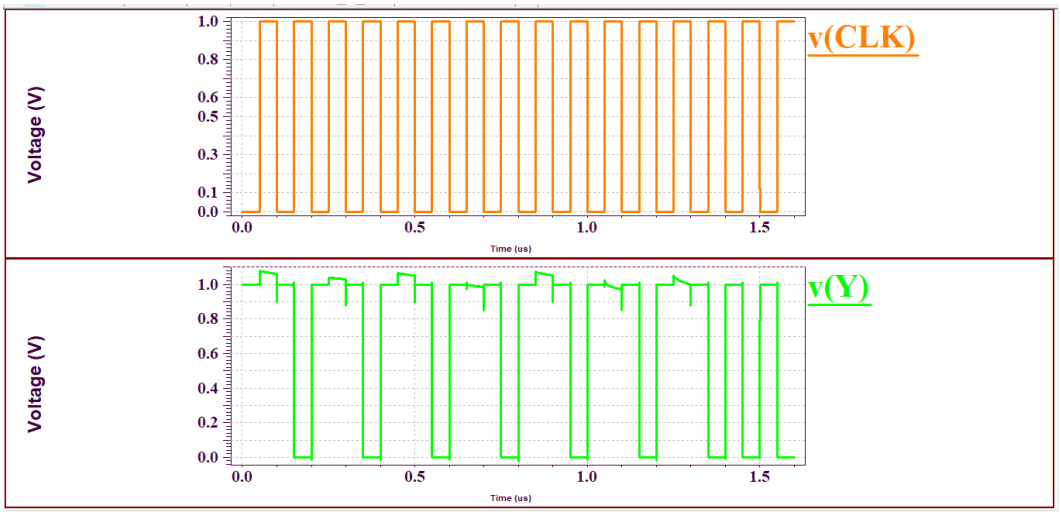


**Fig.5b: Waveforms corresponds to the clock signal and output Y context to dynamic CMOS design**

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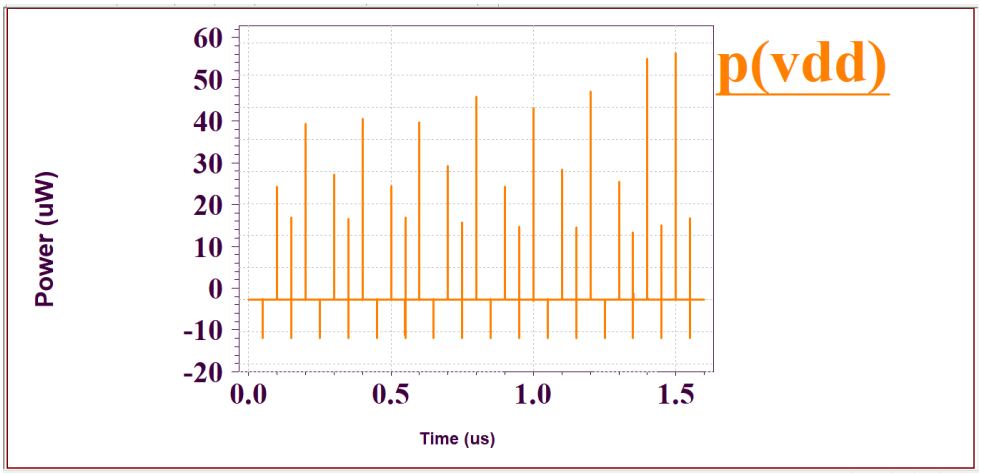


**Fig.6: Instantaneous power dissipation of the dynamic CMOScircuit for the function Y $= \overline{ABC + D}$**

## II. Analysis of Average Power Consumption and Gate Delay of the Circuit Based on the Function $Y = \overline{ABC + D}$

In this section the analysis of average power consumption, gate delay and power-delay product (PDP) of the circuit has been carried out for both the design style – static CMOS & dynamic CMOS.

### IIIA. Measurement and Analysis of Average Power Dissipation and Gate Delay of the Circuit through Static CMOS Design

The Measurement value of Average Power Consumption, gate-delay and PDP of the circuit designed using static CMOS style has been presented in Table-2. The graphical representation of power consumption, gate-delay and PDP are shown in Fig. 7, Fig.8, Fig.9 respectively. It is

**Table 2. Measurement value of Average Power Consumption, Gate-Delay and PDP**

| $V_{DD}$(V) | Average Power Consumption (nW) | Gate Delay (ps) | PDP (aJ) |
|---|---|---|---|
| 0.5 | 5.4 | 59.5 | 0.321 |
| 0.6 | 8.1 | 42.0 | 0.341 |
| 0.7 | 11.2 | 31.9 | 0.358 |
| 0.8 | 14.6 | 23.4 | 0.343 |
| 0.9 | 18.9 | 19.3 | 0.365 |
| 1 | 24.9 | 15.7 | 0.391 |
| 1.1 | 33.2 | 12.1 | 0.402 |
| 1.2 | 44.7 | 9.1 | 0.407 |

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found that as power supply voltage ($V_{DD}$) increases, the power consumption increases but delay decreases. Therefor to get optimum point, the PDP has been plotted and has touched one optimum point around at $V_{DD}$ = 0.8 V.

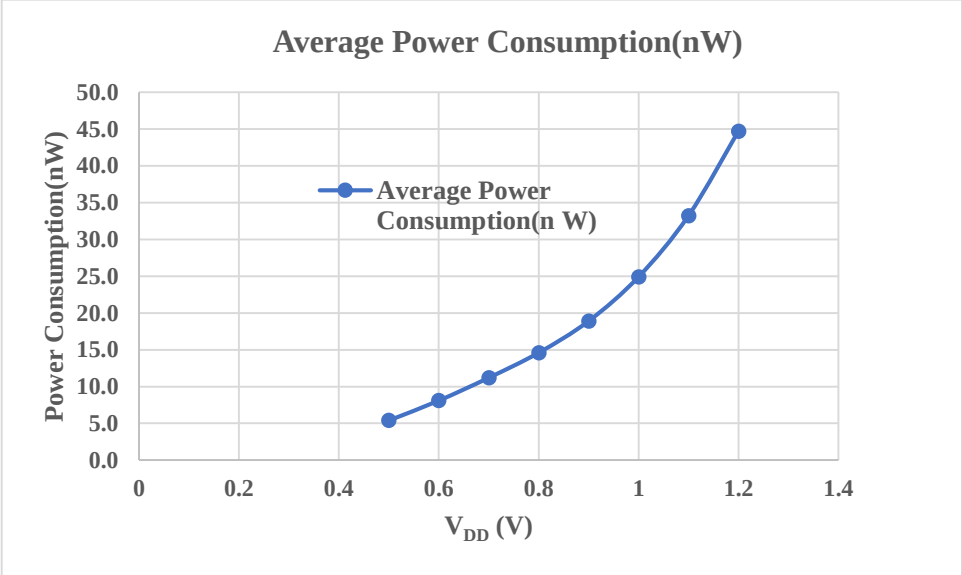


**Fig.7: Average power consumption vs. $V_{DD}$ following static CMOS design**

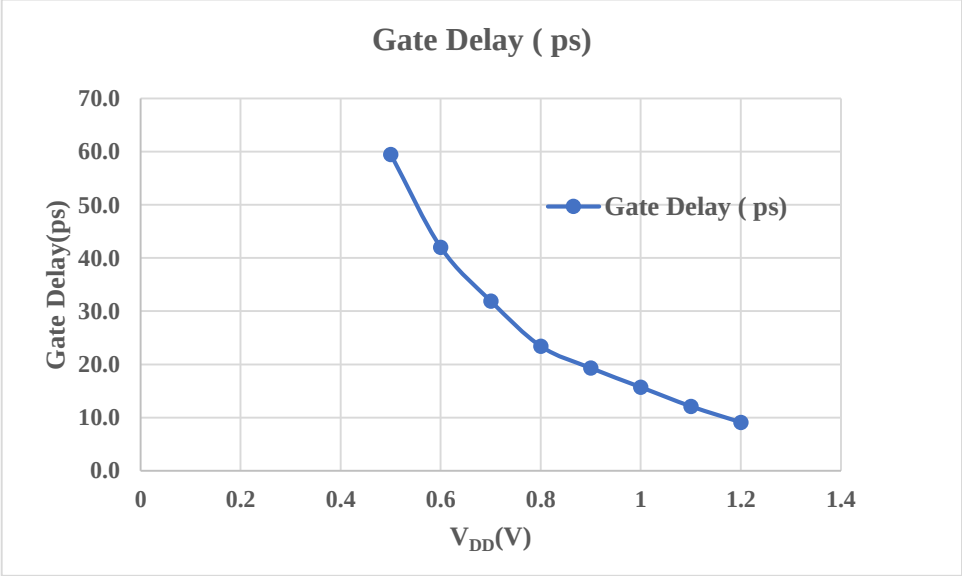


**Fig.8: Gate delay vs. $V_{DD}$ following static CMOS design**

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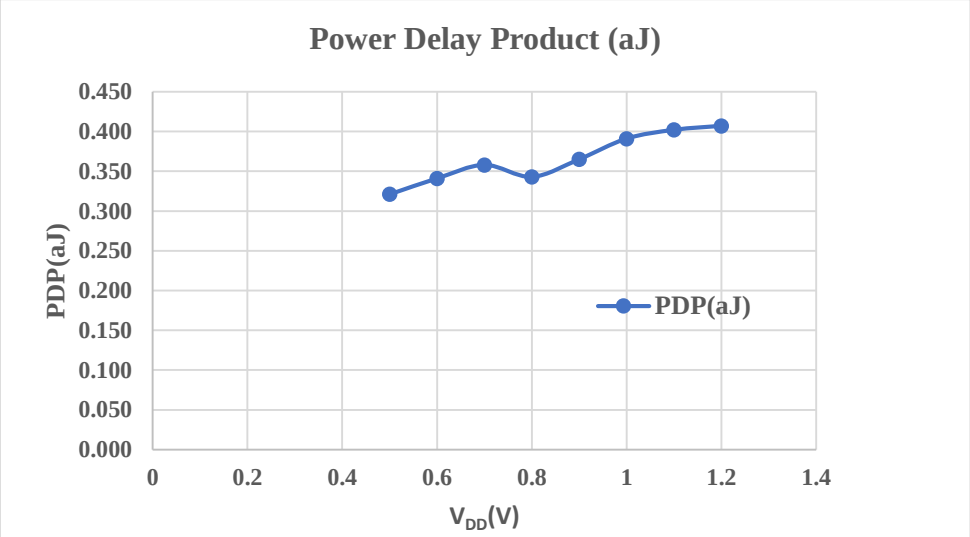


**Fig.9: PDP vs. $V_{DD}$ following static CMOS design**

### IIIB. Measurement and Analysis of Average Power Dissipation and Gate Delay of the Circuit through Dynamic CMOS Design

The Measurement value of Average Power Consumption, gate-delay and PDP of the circuit designed using dynamic CMOS style has been presented in Table-3. The graphical representation of power consumption, gate-delay and PDP are shown in Fig. 10, Fig.11, Fig.12 respectively. It is found that as power supply voltage ($V_{DD}$) increases, the power consumption increases but delay decreases. Therefor to get optimum point, the PDP has been plotted and has touched one optimum point around at $V_{DD}$ = 0.9 V.

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**Table 3. Measurement value of Average Power Consumption, Gate-Delay and PDP**

| $V_{DD}$(V) | Average Power Consumption ( nW) | Gate Delay (ps) | PDP (aJ) |
|---|---|---|---|
| 0.5 | 5.2 | 90.1 | 0.468 |
| 0.6 | 7.9 | 60.9 | 0.481 |
| 0.7 | 11.4 | 44.5 | 0.507 |
| 0.8 | 14.6 | 35.2 | 0.514 |
| 0.9 | 18.4 | 27.3 | 0.502 |
| 1 | 23.8 | 22.7 | 0.541 |
| 1.1 | 31.0 | 19.0 | 0.590 |
| 1.2 | 40.9 | 15.8 | 0.651 |

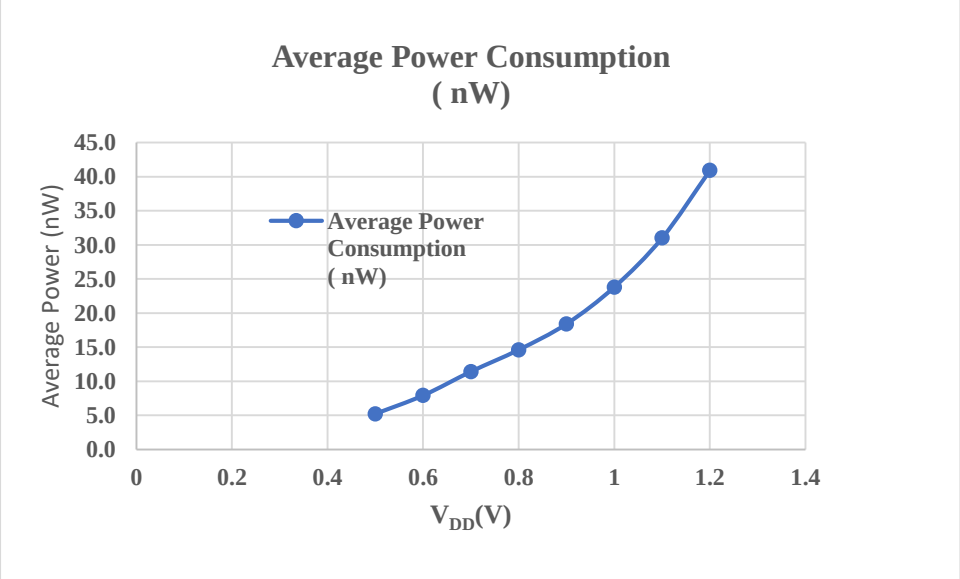


**Fig.10: Average power consumption vs. $V_{DD}$ following dynamic CMOS design**

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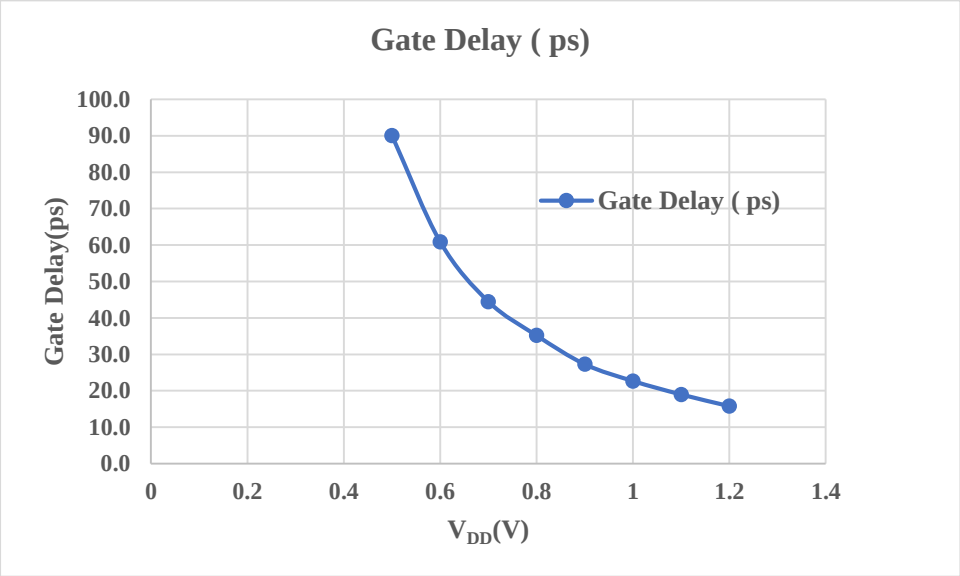


**Fig.11: Gate delay vs. $V_{DD}$ following dynamic CMOS design**

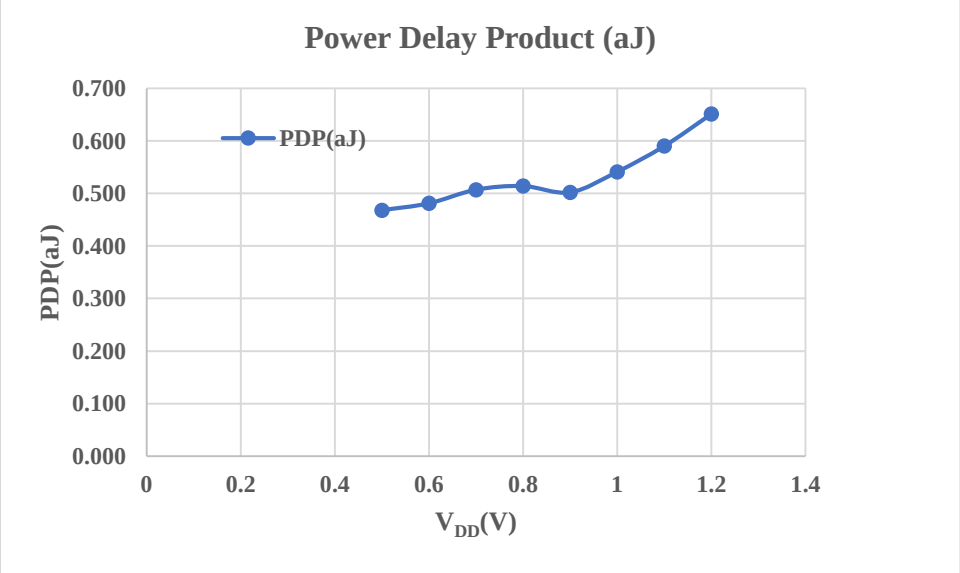


**Fig.12: PDP vs. $V_{DD}$ following dynamic CMOS design**

### IIIC. Comparison of Average Power Dissipation, Gate Delay and PDP of the Circuit through Static and Dynamic CMOS Design

From the measurement valuesas presented in Table-2 and Table-3, it has been found that, for this work, the average power consumption in static CMOS design is little bit higher than dynamic CMOS design. On the other hand, the gate delay is higher in

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case of dynamic CMOS design compared to static CMOS design. Moreover, the PDP vale is higher in case of dynamic CMOS design style.

## Conclusion

In this work one circuit based on the function$Y = \overline{ABC + D}$has been successfully designed using both the static and dynamic CMOS method. The number of transistors in the design using static CMOS is higher than the dynamic CMOS. The average power consumption, gate delay and PDP analysis has been carried out. From the result analysis and recent trends of low power circuit, it can be concluded that the circuit designed using both the methods -static & dynamic CMOS, can be used as a prototype design for low power and high-speed integrated circuit design.

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